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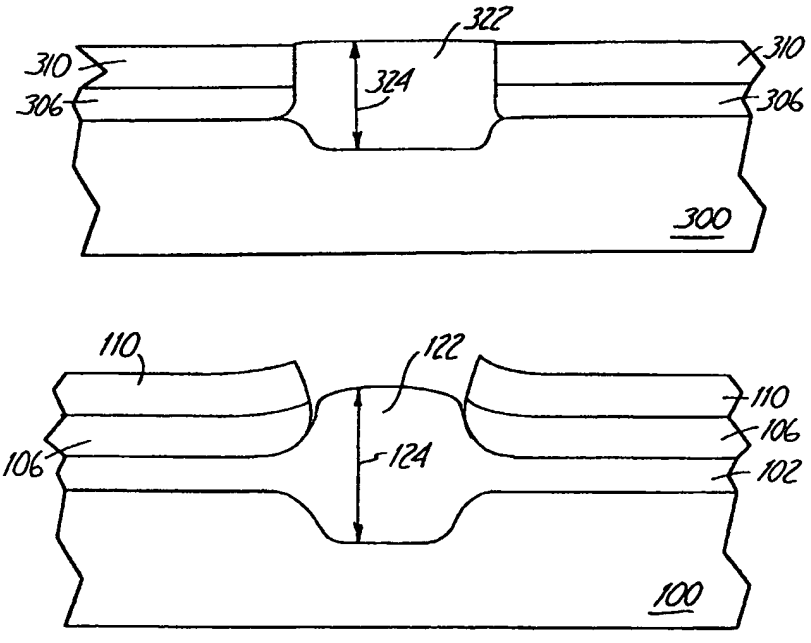
(54) Title: PROCESS OF ISOLATION IN INTEGRATED CIRCUIT FABRICATION, USING AN ANTIREFLECTIVE COATING

(57) Abstract

A method of forming an oxidation diffusion barrier stack for use in fabrication of integrated circuits includes forming an inorganic antireflective material layer (306) on a semiconductor substrate assembly (300) with an oxidation diffusion barrier layer (310) then formed on the inorganic antireflective material layer. Another method of forming such a stack includes forming a pad oxide layer (102) on the semiconductor substrate assembly (100) with an inorganic antireflective material layer (106) then formed on the pad oxide layer and an oxidation diffusion barrier layer (110) formed on the antireflective material layer. Another method of forming the stack includes forming a pad oxide layer (202) on the semiconductor substrate assembly (200). A first oxidation diffusion barrier layer (226) is then formed on the pad oxide layer, an inorganic antireflective material layer (206) is formed on the first oxidation diffusion barrier layer (210), and a second oxidation diffusion barrier layer is formed on the inorganic antireflective material layer. The antireflective material layer may include a layer of material selected from the group of silicon nitride, silicon oxide, and silicon oxynitride and further may be a silicon-rich layer. The oxidation diffusion barrier stacks may be used for oxidation of field regions for isolation in an integration circuit. Further, the various oxidation diffusion barrier stacks are also described.



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PROCESS OF ISOLATION IN INTEGRATED CIRCUIT FABRICATION, USING AN ANTIREFLECTIVE COATING

Field of the Invention

The present invention relates to the fabrication of integrated circuits. More particularly, the present invention relates to the use of antireflective layers in isolation processes.

Background of the Invention

One of the most important processes in the fabrication of semiconductor integrated circuits (ICs) is photolithography. Optical photolithography involves reproducing an image from an optical mask in a layer of photoresist that is supported by underlying layers of a semiconductor substrate assembly. Photolithography is one of the most complicated and critical processes in the fabrication of ICs. The ability to reproduce precise images in a photoresist is crucial to meeting demands for increasing device density.

In the photolithographic process, first, an optical mask is positioned between a radiation source and the photoresist layer on the underlying layers. The radiation source can be, for example, visible light or ultraviolet radiation. Then, the image is reproduced by exposing the photoresist to radiation through the optical mask. Portions of the mask contain an opaque layer, such as, for example, chromium, that prevents exposure of the underlying photoresist. Remaining portions of the mask are transparent, allowing exposure of the underlying photoresist.

The layers underlying the photoresist layer, generally include one or more individual layers that are to be patterned. That is, when a layer is patterned, material from the layer is selectively removed. The ability to pattern layers of material enables ICs to be fabricated. In other words, the patterned layers are used as building blocks in individual devices of the IC. Depending on the type of photoresist utilized (i.e., positive type or negative type), exposed photoresist is either removed when the substrate is contacted with a developer solution, or the exposed

photoresist becomes more resistant to dissolution in the developer solution. Thus, a patterned photoresist layer is able to be formed on underlying layers.

One of the problems experienced with conventional optical photolithography is the difficulty of obtaining uniform exposure of photoresist underlying transparent portions of the mask. It is desired that the light intensity exposing the photoresist be uniform to obtain optimum results.

When sufficiently thick layers of photoresist are used, the photoresist must be (or become) partially transparent upon exposure, so that photoresist at the surface of underlying layers is exposed to a substantially similar extent as the photoresist at the outer surface. Often, however, light that penetrates the photoresist is reflected back toward the light source from the surface of the underlying layers of the substrate assembly. The angle at which the light is reflected is dependent on the topography of the surface of the underlying layers and the type of material of the underlying layers. The reflected light intensity can vary in the photoresist throughout its depth or partially though its depth, leading to nonuniform exposure and undesirable exposure of the photoresist. Such exposure of the photoresist can lead to poorly controlled features (e.g., gates, metal lines, etc.) of the IC.

In an attempt to minimize the variable reflection of light in a photoresist layer, antireflective coatings have been utilized between the underlying layers of a substrate assembly and the photoresist layer or between the photoresist layer and the radiation source. Such antireflective coatings minimize photoresist exposure from surface reflections, allowing exposure across a photoresist layer to be controlled more easily from the radiation incident on the photoresist from the radiation source.

Typically, antireflective coatings are organic materials. Organic layers can, however, lead to particle contamination in the integrated circuit (IC) due to the incomplete removal of organic material from the underlying layers after the photolithography step is performed. Such particle contamination can potentially be detrimental to the electrical performance of the IC. Further, the underlying layers upon which the organic materials are formed may be uneven resulting in different thicknesses of the organic material used as the antireflective coating, e.g., thicker

regions of the organic material may be present at various locations of the underlying layers. As such, when attempting to remove such organic material, if the etch is stopped when the underlying layers are reached, then some organic material may be left. If the etch is allowed to progress to etch the additional thickness in such regions or locations, then the underlying layers may be undesirable etched (e.g., punchthrough of an underlying layer may occur).

Inorganic antireflective layers have also recently been introduced. For example, silicon-rich silicon dioxide, silicon-rich nitride, and silicon-rich oxynitride have been utilized as inorganic antireflective layers. Such inorganic antireflective layers have been utilized, for example, in the patterning of metal lines and polysilicon gates.

After a patterned photoresist layer is formed on a substrate, many other processes are typically performed in the fabrication of ICs. For example, the photoresist can act as an implantation barrier during an implant step. The photoresist can also be utilized to define the outer perimeter of an area (e.g., a contact hole) that is etched in the substrate or individual layers therein. Once again, the photoresist acts as a barrier during the etching process.

One common photolithographic process involves utilizing the patterned photoresist layer over a pad oxide layer and silicon nitride layer on a supporting substrate. The pad oxide layer is utilized as a stress buffer due to the volumetric increase of adjacent growing oxide and the large difference in thermal expansion coefficients of the silicon wafer and the silicon nitride layer that are problematic during subsequent thermal oxidation. The patterned photoresist layer is utilized to selectively remove the pad oxide layer and silicon nitride layer (e.g., LPCVD silicon nitride) in field regions of a substrate.

After such field regions are defined by the remaining regions of the pad oxide layer and the silicon nitride layer, the patterned photoresist layer is removed. Then, the field regions of the substrate are oxidized, for example, using a wet oxidation process, to form field oxide in the field regions. The silicon nitride layer acts as a barrier to oxygen diffusion, preventing oxidation in underlying active regions. This technique is well known as the LOCOS (Local Oxidation of Silicon)

process. One recurring problem, however, with the LOCOS process is encroachment of field oxide under the edges of the silicon nitride in the active regions. This is often referred to as the "bird's beak" phenomenon. As device density increases, the bird's beak problem becomes more problematic because the active region containing the bird's beak is essentially unusable for the fabrication of devices.

Another well known electrical isolation technique is trench isolation. In trench isolation, a trench is etched in the substrate and then filled with deposited oxide. Trench isolation is referred to as shallow trench isolation (STI) or deep trench isolation (DTI), depending on the depth of the trench etched in the substrate. After the oxide is deposited to fill the trench, it is patterned so that the oxide is removed from areas of the substrate outside of the trench etched in the substrate. Conventional photolithography is utilized to pattern the oxide.

Summary of the Invention

There is a need for methods of forming isolation regions for integrated circuits that are well-controlled. One way in which such processes can be better controlled is through improvement of the photolithographic steps used therein. For example, it is desirable to obtain a uniform level of exposure of photoresist used in patterning steps. The present invention provides various methods and structures using inorganic antireflective layers.

A method of forming an oxidation diffusion barrier stack for use in fabrication of integrated circuits in accordance with the present invention includes providing a semiconductor substrate assembly and forming an inorganic antireflective material layer on the semiconductor substrate assembly. An oxidation diffusion barrier layer is then formed on the inorganic antireflective material layer.

Another method of forming an oxidation diffusion barrier stack for use in the fabrication of integrated circuits in accordance with the present invention includes providing a semiconductor substrate assembly and forming a pad oxide layer on the semiconductor substrate assembly. An inorganic antireflective material

layer is then formed on the pad oxide layer and an oxidation diffusion barrier layer is formed on the antireflective material layer.

In yet another method of forming an oxidation diffusion barrier stack for use in the fabrication of integrated circuits in accordance with the present invention includes providing a semiconductor substrate assembly and forming a pad oxide layer on the semiconductor substrate assembly. A first oxidation diffusion barrier layer is then formed on the pad oxide layer, an inorganic antireflective material layer is formed on the first oxidation diffusion barrier layer, and a second oxidation diffusion barrier layer is formed on the inorganic antireflective material layer.

In various embodiments of the methods, the semiconductor substrate assembly is a silicon substrate; the antireflective material layer includes a layer of material selected from the group of silicon nitride, silicon oxide, and silicon oxynitride; the antireflective material layer is a silicon-rich layer; the antireflective material has an index of refraction of about 1.7 to about 3.0; the antireflective material layer has an absorptive coefficient of about 0.2 to about 2.0; and/or the oxidation diffusion barrier layers may be layers of silicon nitride or silicon oxynitride.

Further, a method for use in forming isolation for an integrated circuit is provided. The method includes providing a semiconductor substrate and forming an oxidation diffusion barrier stack on the semiconductor substrate. The oxidation diffusion barrier stack includes an inorganic antireflective material layer. The oxidation diffusion barrier stack is patterned resulting in exposed regions of the semiconductor substrate and the exposed regions of the semiconductor substrate are oxidized.

An oxidation diffusion barrier stack in accordance with the present invention includes an inorganic antireflective material layer formed on a semiconductor substrate assembly and an oxidation diffusion barrier layer formed on the inorganic antireflective material layer.

Another oxidation diffusion barrier stack in accordance with the present invention includes a pad oxide layer formed on a semiconductor substrate,

an oxidation diffusion barrier layer, and an inorganic antireflective material layered between the pad oxide and the oxidation diffusion barrier layer.

Yet another oxidation diffusion barrier stack in accordance with the present invention includes a first oxidation diffusion barrier layer, a second oxidation diffusion barrier layer, and an inorganic antireflective material layered between the first and second oxidation diffusion barrier layers.

In various embodiments of the stacks, the inorganic antireflective material may be selected from the group of silicon-rich silicon oxide, silicon-rich silicon nitride, and silicon-rich silicon oxynitride; and/or oxidation diffusion barrier layers may be silicon nitride layers or silicon oxynitride layers.

Brief Description of the Drawing

The following figures are provided for ease of description and understanding of the invention. Thus, scaling and dimensions in the figures are not exact.

Figure 1A is a cross-sectional representation of a pad oxide layer supported by a semiconductor substrate.

Figure 1B is a cross-sectional representation of the structure of Fig. 1A, wherein an inorganic antireflective coating is formed thereon in accordance with the present invention.

Figure 1C is a cross-sectional representation of the structure of Fig. 1B, wherein a silicon nitride is formed thereon.

Figure 1D is a cross-sectional representation of the structure of Fig. 1C, wherein a photoresist layer is formed thereon to pattern the underlying material.

Figure 1E is a cross-sectional representation of the structure of Fig. 1D, wherein the underlying stack of silicon nitride, antireflective coating, and pad oxide layers have been patterned.

Figure 1F is a cross-sectional representation of the structure of Fig. 1E, wherein field oxide is formed in field regions of the substrate between the patterned stack.

Figure 2A is a cross-sectional representation of a pad oxide layer supported by a semiconductor substrate.

Figure 2B is a cross-sectional representation of the structure of Fig. 2A, wherein a first silicon nitride layer is formed thereon.

Figure 2C is a cross-sectional representation of the structure of Fig. 2B, wherein an antireflective layer is formed thereon.

Figure 2D is a cross-sectional representation of the structure of Fig. 2C, wherein a second silicon nitride layer is formed thereon.

Figure 2E is a cross-sectional representation of the structure of Fig. 2D, wherein a photoresist layer is formed thereon to pattern the underlying material.

Figure 2F is a cross-sectional representation of the structure of Fig. 2E, wherein the underlying stack of second silicon nitride, antireflective, first silicon nitride and pad oxide layers have been patterned.

Figure 2G is a cross-sectional representation of the structure of Fig. 2F, wherein field oxide is formed in field regions of the substrate between the patterned stack.

Figure 3A is a cross-sectional representation of an antireflective layer supported by a semiconductor substrate.

Figure 3B is a cross-sectional representation of the structure of Fig. 3A, wherein a silicon nitride layer is formed thereon.

Figure 3C is a cross-sectional representation of the structure of Fig. 3B, wherein a photoresist layer is formed thereon to pattern the underlying material.

Figure 3D is a cross-sectional representation of the structure of Fig. 3C, wherein the underlying stack of antireflective coating and silicon nitride layers have been patterned.

Figure 3E is a cross-sectional representation of the structure of Fig. 3D, wherein field oxide is formed in field regions of the substrate between the patterned stack.

Figures 4A and 4B are cross-sectional representations of a method of trench isolation in accordance with the present invention.

Detailed Description of the Embodiments

To provide better controlled photolithography when forming electrical isolation in an integrated circuit (IC), an antireflective coating (ARC) is used. Using an ARC results in uniform exposure to photoresist which has been formed on underlying layers of a substrate assembly. Thus, well-defined patterns are able to be reproduced in the photoresist. Forming well-defined patterns in the photoresist leads to well-defined patterning of underlying material. As device density is increasing, such precise definition is becoming increasingly important.

It is to be understood that the term substrate assembly, as used herein, includes a wide variety of semiconductor-based structures, including but not limited to a semiconductor substrate and a semiconductor substrate having one or more layers, regions formed thereon or therein. Semiconductor substrates can be a single layer of material, such as a silicon wafer or is understood to include silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor, as well as other semiconductor substrate structures. When reference is made to a semiconductor substrate assembly in the following description, various process steps may have been utilized to form regions/junctions in a semiconductor substrate or may have been used to form one or more layers or regions of material relative to the substrate.

ARCs according to the present invention are preferably inorganic. Such preferred inorganic ARCs are formed between a photoresist layer and underlying layers for use in photolithography. Suitable ARC materials according to the present invention include a nonstoichiometric silicon-rich oxide, silicon-rich nitride, and silicon-rich oxynitride. A preferred chemical formula of the silicon-rich oxide is SiO_x, where x is in the range of about 0.3 to about 1.9. A preferred chemical formula of the silicon-rich nitride is SiN_y, where y is in the range of about 0.2 to about 1.0. A preferred chemical formula of the silicon-rich oxynitride is SiO_xN_y, where x is in the range of about 0.2 to about 1.9 and y is in the range of about .01 to about 1.0.

Further, suitable ARC materials generally have an index of refraction of about 1.7 to about 3.0 and an absorptive coefficient of about 0.2 to about 2.0 at a wavelength of about 248 nanometers. Preferably, the index of refraction is about 2.0 to about 2.7 and the absorptive coefficient is about 0.4 to about 1.5 at a wavelength of about 248 nanometers. The absorptive coefficient needed depends on the index of refraction and the absorptive coefficient of the photoresist and other underlying layers of the substrate assembly upon which the photoresist is formed, as well as the dimensions of the underlying substrate assembly features and layers. Depending on the wavelength, as the amount of silicon in the nonstoichiometric ARC materials increase, the index of refraction and the absorptive coefficient of the ARC material typically increase as well. For example, this is generally the case for a wavelength of about 365 nanometers.

A layer of ARC material is formed on a substrate assembly using chemical vapor deposition (CVD). Preferably, plasma-enhanced chemical vapor deposition (PECVD) is used. PECVD allows formation of the layer at relatively low temperatures of about 400°C. By controlling flow rates of certain precursor gases, material of the desired stoichiometry can be formed on the substrate. For example, when more of a particular component is desired in the resulting material, the flow rate of the precursor gas of that component is increased or the flow rate of the other precursor gas(es) is decreased.

Silicon-rich oxide is formed by flowing a silicon-containing precursor gas and an oxygen-containing precursor gas in a process chamber. Typically, an inert carrier gas, for example, argon or helium, is used as well. The silicon-containing precursor gas may be any member of the silane family (e.g., silane, disilane, dichlorosilane, etc.). Preferably, the oxygen-containing precursor gas is nitrous oxide (N_2O); however, other oxygen-containing precursors, including O_2, NO, N_2O_2, and NO_2, may be utilized.

Silicon-rich nitride is formed by flowing a silicon-containing precursor gas and a nitrogen-containing precursor gas in a process chamber. Typically, a carrier gas, for example, nitrogen, is used as well. The silicon-containing precursor gas may be any member of the silane family (e.g., silane,

disilane, dichlorosilane, etc.). Preferably, the nitrogen-containing precursor gas is ammonia (NH_3); however, other nitrogen-containing precursor gases, such as nitrogen or a gas from the family of $[C_nH_{2n+1}]_2NH$ (e.g., $[CH_3]_2NH$), may be used.

Silicon-rich oxynitride is formed by flowing a silicon-containing precursor gas, an oxygen-containing precursor gas, and a nitrogen-containing precursor gas in a process chamber. Typically, a carrier gas, for example, nitrogen, is used as well. The silicon-containing precursor gas may be any member of the silane family (e.g., silane, disilane, dichlorosilane, etc.). Preferably, the oxygen-containing precursor gas is nitrous oxide (N_2O); however, for example, O_2, NO, N_2O_2, and NO_2, may be used. Preferably, the nitrogen-containing precursor gas is ammonia (NH_3); however, for example, nitrogen or a gas from the family of $[C_nH_{2n+1}]_2NH$, may be used.

When using an ARC material according to the present invention, a layer of the ARC material is formed in an oxidation diffusion barrier stack. Typically, the oxidation diffusion barrier stack is formed as a blanket layer over the supporting semiconductor structure. A layer of photoresist is then formed over the oxidation diffusion barrier stack. The photoresist is then exposed using conventional photolithography. After the photoresist is contacted with a developer solution, photoresist is selectively removed from the substrate surface according to the pattern exposed therein.

Next, the oxidation diffusion barrier stack is selectively etched in regions where the photoresist has been removed therefrom to pattern the stack. The etchant is selected according to the materials in the oxidation diffusion barrier stack. Preferably, a dry etch is used due to the ability of dry etchants to etch anisotropically. The various oxide and nitride layers described herein can be etched using any suitable etching technique. For example, reactive ion etching using a fluorine chemistry may be used to etch oxides and nitrides, e.g., a chemistry using a CHF_3 or CF_4. The type of gas flow can be easily controlled in a plasma reactor by selectively opening and closing mass controllers coupled to the plasma reactor. Thus, if the oxidation diffusion barrier stack includes more than one type of

material, the stack can be etched in-situ due to the ability to selectively control the flow of gas.

Once the oxidation diffusion barrier stack is patterned, the exposed portions of the semiconductor substrate assembly (e.g., doped silicon, undoped silicon) can be oxidized. For field oxidation, wet oxidation is typically utilized to perform the oxidization. This process is well known to one of ordinary skill in the art. In such a process, for example, the substrate is placed in a furnace, ramped to a temperature of about 900°C to about 1,150°C. Once the desired thickness of field oxide is grown, the temperature of the furnace is decreased and the substrate is removed from the furnace.

After the oxidation process, the patterned oxidation diffusion barrier stack is typically removed. Once again, a dry etch, as described above, is utilized.

In one embodiment of the present invention, the oxidation diffusion barrier stack is supported by a silicon wafer. As illustrated in Fig. 1A, a pad oxide layer 102 is formed on the silicon wafer 100. The silicon wafer 100 is typically doped (i.e., n-type or p-type), but it is not necessary for the practice of this invention. The thickness 104 of the pad oxide layer 102 is typically about a few hundred angstroms or less.

Next, as illustrated in Fig. 1B, an ARC layer 106 is formed on the pad oxide layer 102. The thickness 108 of the ARC layer 106 is preferably about 100Å to about 500Å. More preferably, the thickness 108 of the ARC layer 106 is about 250Å to about 350Å. Depending on the wavelength of incident radiation during photolithography and the dimensions of the oxidation diffusion barrier stack, however, the thickness 108 of the ARC layer 106 can vary.

Then, as illustrated in Fig. 1C, a silicon nitride layer 110 is formed on the ARC layer 106. The thickness 112 of the silicon nitride layer 110 is preferably about 3000 Å or less. More preferably, the thickness 112 of the silicon nitride layer 110 is about 1000 Å to about 2400 Å. The silicon nitride layer 110 is preferably formed using low pressure chemical vapor deposition (LPCVD), for example, at a temperature of about 500°C to about 750°C. It is to be appreciated that, while a silicon nitride layer is utilized in this illustration for the purpose of an oxidation

diffusion material, any material known to prevent (or minimize) the diffusion of oxygen therethrough can be utilized in place of, or in addition to, the silicon nitride layer 110. For example, silicon oxynitride, boron nitride, and aluminum nitride may be used.

Next, as illustrated in Fig. 1D, a photoresist layer 114 is formed on the silicon nitride layer 110. The thickness 116 of the photoresist layer 114 is typically about 7000 Å to about 10,000 Å. The minimum thickness 116 of the photoresist layer 114 is governed by the need to have the patterned photoresist layer 114 remain after a subsequent etching step, when the oxidation diffusion barrier stack is selectively removed from the silicon wafer 100 in exposed regions underlying the patterned photoresist layer.

The oxidation diffusion barrier stack is etched according to the technique previously described and the photoresist layer 114 is removed, resulting in the structure illustrated in Fig. 1E. The photoresist layer 114 is removed according to well known methods to one of ordinary skill in the art. For example, an oxygen ash can be used to remove the photoresist layer 114. Regions where the oxidation diffusion barrier stack is etched to the underlying silicon wafer 100 are field regions 118. Regions where the patterned oxidation diffusion barrier stack remains on the silicon wafer 100 are active regions 120. Individual or multiple active devices can subsequently be formed in the active regions 120 of the substrate 100, as is readily known to one skilled in the art.

Field oxide 122 is then formed in the field regions 118, resulting in the structure illustrated in Fig. 1F. The thickness 124 of the field oxide 122 is governed by the device density and operating voltages of individual devices later formed in the active regions 120 illustrated in Fig. 1E. Typically, the thickness 124 of the field oxide 122 is about a few thousand angstroms. The thickness 124 of the field oxide 122, however, is not critical to the practice of this invention.

In another embodiment of the invention, a pad oxide layer 202 is formed on the silicon wafer 200, as illustrated in Fig. 2A. The silicon wafer 200 is typically doped (i.e., n-type or p-type), but it is not necessary for the practice of this

invention. The thickness 204 of the pad oxide layer 202 is typically about a few hundred angstroms or less.

Next, as illustrated in Fig. 2B, a first silicon nitride layer 226 is formed on the pad oxide layer 202. The thickness 228 of the first silicon nitride layer 226 is preferably small enough that the first silicon nitride layer 226 does not delaminate from the pad oxide layer 202. More preferably the thickness 228 of the first silicon nitride layer 226 is about 1,500Å or less. Even more preferably, the thickness 228 of the first silicon nitride layer 226 is about 50 Å to about 1,500 Å. Most preferably, the thickness 228 of the first silicon nitride layer 226 is about 300 Å to about 1000 Å. The first silicon nitride layer 226 can be formed using techniques well known to one of ordinary skill in the art. Preferably, one of PECVD and LPCVD is used to form the first silicon nitride layer 226. More preferably, PECVD is used.

Then, an ARC layer 206 is formed on the first silicon nitride layer 226, as illustrated in Fig. 2C. The thickness 208 of the ARC layer 206 is about 100Å to about 500Å. Preferably, the thickness 208 of the ARC layer 206 is about 200 Å to about 350Å. Depending on the wavelength of incident radiation during photolithography and the dimensions of the oxidation diffusion barrier stack, however, the thickness 208 of the ARC layer 206 can vary.

Then, as illustrated in Fig. 2D, a second silicon nitride layer 210 is formed on the ARC layer 206. The thickness 212 of the second silicon nitride layer 210 is preferably about 3,000Å or less. More preferably, the thickness 212 of the second silicon nitride layer 210 is selected such that a total thickness of the first and second silicon nitride layers 226 and 210, respectively, is about 1,000Å to about 2,000Å. The second silicon nitride layer 110 is preferably formed using low pressure chemical vapor deposition (LPCVD). It is to be appreciated that, while silicon nitride is utilized for the first and second silicon nitride layers in this illustration for the purpose of an oxidation diffusion material, any material known to prevent (or minimize) the diffusion of oxygen therethrough can be utilized in place of, or in addition to, the first and second silicon nitride layers 226 and 210.

Next, as illustrated in Fig. 2E, a photoresist layer 214 is formed on the second silicon nitride layer 210. The thickness 216 of the photoresist layer 214 is typically about a few thousand angstroms. The minimum thickness 216 of the photoresist layer 214 is governed by the need to prevent removal of the photoresist layer 214 through to the underlying layer during a subsequent etching step, where the oxidation diffusion barrier stack is selectively removed from the silicon wafer 200 in exposed regions underlying the photoresist layer 214.

The oxidation diffusion barrier stack is etched according to the technique previously described and the photoresist layer 214 is removed, resulting in the structure illustrated in Fig. 2F. The photoresist layer 214 is removed according to well known methods to one of ordinary skill in the art. For example, an oxygen ash can be used to remove the photoresist layer 214. Regions where the oxidation diffusion barrier stack is etched to the underlying silicon wafer 200 are field regions 218. Regions where the patterned oxidation diffusion barrier stack remains on the silicon wafer 200 are active regions 220. Individual or multiple active devices can subsequently be formed in the active regions 220 of the substrate 200.

Field oxide 222 is then formed in the field regions 218, resulting in the structure illustrated in Fig. 2G. The thickness 224 of the field oxide 222 is governed by the device density and operating voltages of individual devices later formed in the active regions 220 illustrated in Fig. 2F. Typically, the thickness 224 of the field oxide 222 is about a few thousand angstroms. The thickness 224 of the field oxide 222, however, is not critical to the practice of this invention.

In yet another embodiment, an ARC layer 306 is formed directly on the silicon wafer 300 as illustrated in Fig. 3A. The silicon wafer 300 is typically doped (i.e., n-type or p-type), but it is not necessary for the practice of this invention. The thickness 308 of the ARC layer 306 is about 100Å to about 500Å. Preferably, the thickness 308 of the ARC layer 306 is about 200Å to about 400Å. Depending on the wavelength of incident radiation during photolithography and the dimensions of the oxidation diffusion barrier stack, however, the thickness 308 of the ARC layer 306 can vary.

Then, as illustrated in Fig. 3B, a silicon nitride layer 310 is formed on the ARC layer 306. The thickness 312 of the silicon nitride layer 310 is preferably about 3000 Å or less. More preferably, the thickness 312 of the silicon nitride layer 310 is about 1000 Å to about 2000 Å. The silicon nitride layer 310 is preferably formed using low pressure chemical vapor deposition (LPCVD). It is to be appreciated that, while a silicon nitride layer is utilized in this illustration for the purpose of an oxidation diffusion material, any material known to prevent (or minimize) the diffusion of oxygen therethrough can be utilized in place of, or in addition to, the silicon nitride layer 310.

Next, as illustrated in Fig. 3C, a photoresist layer 314 is formed on the silicon nitride layer 310. The thickness 316 of the photoresist layer 314 is typically about 7000 Å to about 10,000 Å. The minimum thickness 316 of the photoresist layer 314 is governed by the need to prevent removal of the photoresist layer 314 through to the underlying layer during a subsequent etching step, where the oxidation diffusion barrier stack is selectively removed from the silicon wafer 300 in exposed regions underlying the photoresist layer 314.

The oxidation diffusion barrier stack is etched according to the technique previously described and the photoresist layer 314 is removed, resulting in the structure illustrated in Fig. 3D. The photoresist layer 314 is removed according to well known methods to one of ordinary skill in the art. For example, an oxygen ash can be used to remove the photoresist layer 314. Regions where the oxidation diffusion barrier stack is etched to the underlying silicon wafer 300 are field regions 318. Regions where the patterned oxidation diffusion barrier stack remains on the silicon wafer 300 are active regions 320. Individual or multiple active devices can subsequently be formed in the active regions 320 of the substrate 300.

Field oxide 322 is then formed in the field regions 318, resulting in the structure illustrated in Fig. 3E. The thickness 324 of the field oxide 322 is governed by the device density and operating voltages of individual devices later formed in the active regions 320 illustrated in Fig. 3D. Typically, the thickness 324 of the field oxide layer 322 is about a few thousand angstroms. The thickness 324 of the field oxide layer 322, however, is not critical to the practice of this invention.

As compared to the first and second embodiments of the invention, this third embodiment is preferably used when process complexity is a concern. Due to the elimination of the pad oxide layer used in both the first and second embodiments and elimination of the first silicon nitride layer of the second embodiment, process efficiency is increased. The pad oxide layer is not necessary in this third embodiment due to the use of inorganic ARC material of the present invention. Such ARC material provides a lower stress interface with the underlying silicon substrate because it is silicon-rich. Thus, it has been found that a pad oxide layer is not necessary to relieve excess stress at the silicon interface, as is usually seen at the interface between silicon nitride and the silicon wafer.

All patents disclosed herein are incorporated by reference in their entirety, as if individually incorporated. The foregoing detailed description, illustrations, and examples have been given for clarity of understanding only. No unnecessary limitations are to be understood therefrom. The invention is not limited to the exact details shown and described, for variations obvious to one skilled in the art will be included within the invention defined by the claims. For example, while the present invention has been described with reference and illustration supporting a LOCOS process, other isolation techniques can benefit from the use of the present invention. For example, trench isolation (the method for forming such trenches is illustrated in Figures 4A and 4B) can benefit from oxidation diffusion barrier stacks, represented generally as 438, of the present invention. As illustrated in Fig. 4A, in trench isolation, a trench 440 is etched in the substrate assembly 442 through the oxidation diffusion barrier stack 438. The trench 440 is then filled with deposited oxide 444, as illustrated in Fig. 4B. Trench isolation is referred to as shallow trench isolation (STI) or deep trench isolation (DTI), depending on the thickness of the trench etched in the substrate assembly.

As described, the oxidation diffusion barrier stack of the present invention is utilized in the photolithography step that defines regions in the substrate assembly to be etched for providing the trench 440. The method of forming trench isolation includes providing a semiconductor substrate assembly; forming an oxidation diffusion barrier stack having an inorganic antireflective material on the

semiconductor substrate assembly; patterning the oxidation diffusion barrier stack resulting in exposed regions of the semiconductor substrate assembly; etching a trench in the semiconductor substrate assembly as defined by the patterned stack; and depositing oxide in the trench of the semiconductor substrate assembly.

After the oxide is deposited, it is patterned so that it can be removed from areas of the substrate outside of the trench etched in the substrate. Conventional photolithography is utilized to pattern the oxide. Once again, the oxidation diffusion barrier stack of the present invention can be utilized in this photolithography step. A wide variety of other uses are also suitable for use of the present invention.

What is claimed is:

1. A method of forming an oxidation diffusion barrier stack for use in fabrication of integrated circuits, the method comprising the steps of:

providing a semiconductor substrate assembly;

forming an inorganic antireflective material layer on the semiconductor substrate assembly; and

forming an oxidation diffusion barrier layer on the antireflective material layer.

2. The method of claim 1, wherein the semiconductor substrate assembly is a silicon substrate.

3. The method of claim 2, wherein the step of forming the antireflective material layer comprises forming a layer of material selected from the group of silicon nitride, silicon oxide, and silicon oxynitride.

4. The method of claim 3, wherein the step of forming the antireflective material layer comprises forming a silicon-rich layer.

5. The method of claim 1, wherein the step of forming an antireflective material layer comprises forming a layer of silicon-rich silicon oxide.

6. The method of claim 1, wherein the step of forming an antireflective material layer comprises forming a layer of silicon-rich silicon nitride.

7. The method of claim 1, wherein the step of forming an antireflective material layer comprises forming a layer of silicon-rich silicon oxynitride.

8. The method of claim 1, wherein the step of forming an antireflective material layer comprises forming an antireflective material layer having an index of refraction of about 1.7 to about 3.0.

9. The method of claim 8, wherein the step of forming an antireflective material layer comprises forming an antireflective material layer having an absorptive coefficient of about 0.2 to about 2.0.

10. The method of claim 1, wherein the step of forming an antireflective material layer comprises forming an antireflective material layer having an absorptive coefficient of about 0.2 to about 2.0.

11. The method of claim 1, wherein the step of forming an oxidation diffusion barrier layer comprises forming a layer of one of silicon nitride an silicon oxynitride.

12. A method of forming an oxidation diffusion barrier stack for use in the fabrication of integrated circuits, the method comprising the steps of:

providing a semiconductor substrate assembly;

forming a pad oxide layer on the semiconductor substrate assembly;

forming an inorganic antireflective material layer on the pad oxide layer; and

forming an oxidation diffusion barrier layer on the antireflective material layer.

13. The method of claim 12, wherein the semiconductor substrate assembly is a silicon substrate.

14. The method of claim 13, wherein the step of forming an inorganic antireflective material layer comprises forming a layer of material selected from the group of silicon-rich silicon oxide, silicon-rich silicon nitride, and silicon-rich silicon oxynitride.

15. The method of claim 12, wherein the inorganic antireflective material layer is SiO_x, where x is in the range of about 0.3 to about 1.9.

16. The method of claim 12, wherein the inorganic antireflective material layer is SiN_y, where y is in the range of about 0.2 to about 1.0.

17. The method of claim 12, wherein the inorganic antireflective material layer is SiO_xN_y, where x is in the range of about 0.01 to about 1.0.

18. The method of claim 12, wherein the step of forming an oxidation diffusion barrier layer comprises forming a layer of one of silicon nitride and silicon oxynitride.

19. A method of forming an oxidation diffusion barrier stack for use in fabrication of integrated circuits, the method comprising the steps of:

providing a semiconductor substrate assembly;

forming a pad oxide layer on the semiconductor substrate assembly;

forming a first oxidation diffusion barrier layer on the pad oxide layer;

forming an inorganic antireflective material layer on the first oxidation diffusion barrier layer; and

forming a second oxidation diffusion barrier layer on the inorganic antireflective material layer.

20. The method of claim 19, wherein the semiconductor substrate assembly is a silicon substrate.

21. The method of claim 20, wherein the step of forming an inorganic antireflective material layer comprises forming a layer of material selected from the group of silicon-rich silicon oxide, silicon-rich silicon nitride, and silicon-rich silicon oxynitride.

22. The method of claim 21, wherein the inorganic antireflective material layer is SiO_x, where x is in the range of about 0.3 to about 1.9.

23. The method of claim 21, wherein the inorganic antireflective material layer is SiN_y, where y is in the range of about 0.2 to about 1.0.

24. The method of claim 21, wherein the inorganic antireflective material layer is SiO_xN_y, where x is in the range of about 0.01 to about 1.0.

25. The method of claim 19, wherein the steps of forming the first and second oxidation diffusion barrier layers comprises forming the first and second oxidation diffusion layers from materials selected from the group of silicon nitride and silicon oxynitride.

26. A method for use in forming isolation for an integrated circuit, the method comprising the steps of:

providing a semiconductor substrate;

forming an oxidation diffusion barrier stack on the semiconductor substrate, the oxidation diffusion barrier stack comprising an inorganic antireflective material layer;

patterning the oxidation diffusion barrier stack resulting in exposed regions of the semiconductor substrate; and

oxidizing the exposed regions of the semiconductor substrate.

27. The method of claim 26, wherein the step of forming the oxidation diffusion barrier stack comprises the steps of:

forming the inorganic antireflective material layer on the semiconductor substrate; and

forming an oxidation diffusion barrier layer on the inorganic antireflective material layer.

28. The method of claim 26, wherein the step of forming the oxidation diffusion barrier stack comprises the steps of:

forming a pad oxide layer on the semiconductor substrate;

forming the inorganic antireflective material layer on the pad oxide layer; and

forming an oxidation diffusion barrier layer on the inorganic antireflective material layer.

29. The method of claim 26, wherein the step of forming the oxidation diffusion barrier stack comprises the steps of:

forming a pad oxide layer on the semiconductor substrate;

forming a first oxidation diffusion barrier layer on the pad oxide layer;

forming the inorganic antireflective material layer on the first oxidation diffusion barrier layer; and

forming a second oxidation diffusion barrier layer on the inorganic antireflective material layer.

30. The method of claim 26, wherein the step of patterning the oxidation diffusion barrier stack comprises continuously flowing at least a fluorocarbon gas in a plasma reactor containing the oxidation diffusion barrier stack to remove portions of the oxidation diffusion barrier stack.

31. A method for use in forming isolation for an integrated circuit, the method comprising the steps of:

providing a semiconductor substrate assembly;

forming an oxidation diffusion barrier stack comprising an inorganic antireflective material on the semiconductor substrate assembly;

patterning the oxidation diffusion barrier stack resulting in exposed regions of the semiconductor substrate assembly;

etching a trench in the semiconductor substrate assembly through the oxidation diffusion barrier stack; and

depositing an insulating material in the trench of the semiconductor substrate assembly.

32. An oxidation diffusion barrier stack, comprising:

an inorganic antireflective material layer formed on a semiconductor substrate assembly; and

an oxidation diffusion barrier layer formed on the inorganic antireflective material layer.

33. The stack of claim 32, wherein the semiconductor substrate assembly is a antireflective material layer is silicon substrate.

34. The stack of claim 32, wherein the inorganic antireflective material is selected from the group of silicon-rich silicon oxide, silicon-rich silicon nitride, and silicon-rich silicon oxynitride.

35. The stack of claim 32, wherein the oxidation diffusion barrier layer comprises silicon nitride.

36. The stack of claim 32, wherein the inorganic antireflective material has a thickness of about 100 angstroms to about 500 angstroms.

37. The stack of claim 32, wherein the oxidation diffusion barrier layer comprises silicon oxynitride.

38. An oxidation diffusion barrier stack, comprising:

a pad oxide layer formed on a semiconductor substrate;

an oxidation diffusion barrier layer; and

an inorganic antireflective material layered between the pad oxide and the oxidation diffusion barrier layer.

39. The stack of claim 37, wherein the inorganic antireflective material is selected from the group of silicon oxide, silicon nitride, and silicon oxynitride.

40. The stack of claim 38, wherein the inorganic antireflective material is a silicon-rich inorganic antireflective material.

41. An oxidation diffusion barrier stack, comprising:

a first oxidation diffusion barrier layer;

a second oxidation diffusion barrier layer; and

an inorganic antireflective material layered between the first and second oxidation diffusion barrier layers.

42. The stack of claim 40, further comprising a pad oxide layer formed on a substrate assembly, the first oxidation diffusion barrier layer being formed on the pad oxide layer.

43. The stack of claim 41, wherein the inorganic antireflective material is selected from the group of silicon-rich silicon oxide, silicon-rich silicon nitride, and silicon-rich silicon oxynitride.

44. The stack of claim 40, wherein at least one of the first and second oxidation diffusion barrier layers comprises silicon nitride.

45. The stack of claim 40, wherein at least one of the first and second oxidation diffusion barrier layers comprises silicon nitride.

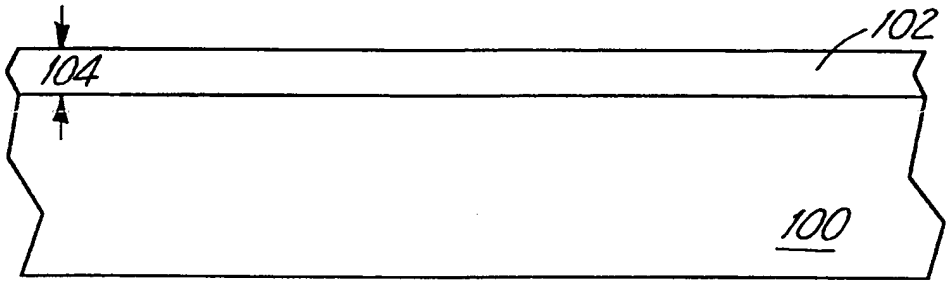

FIG. 1A

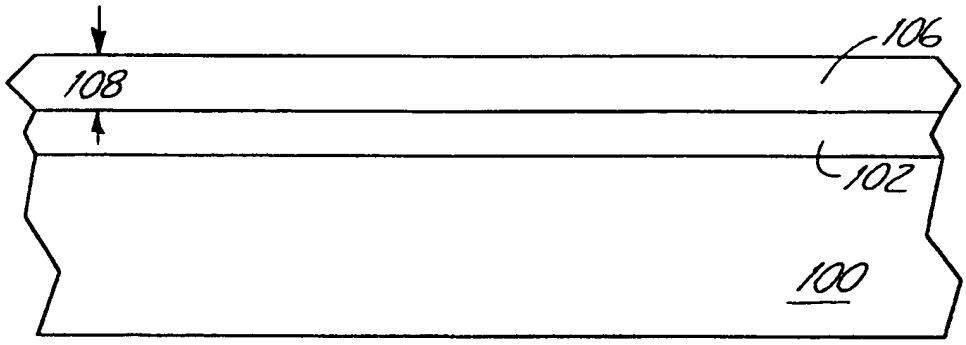

FIG. 1B

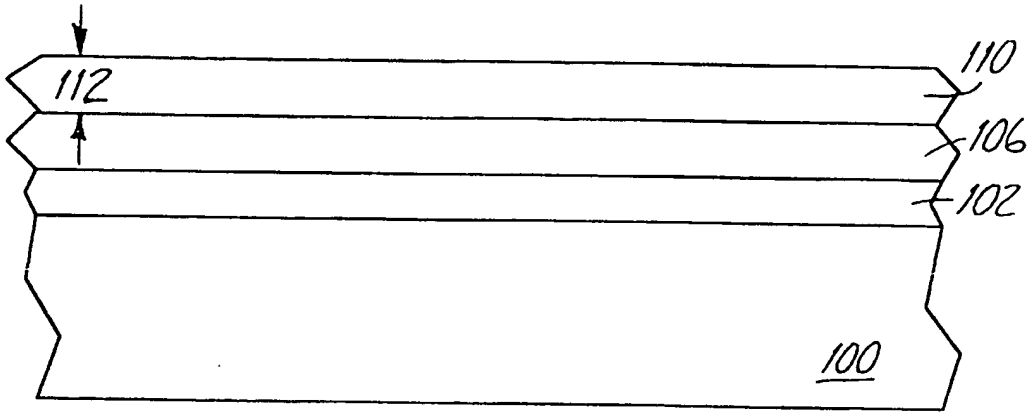

FIG. 1C

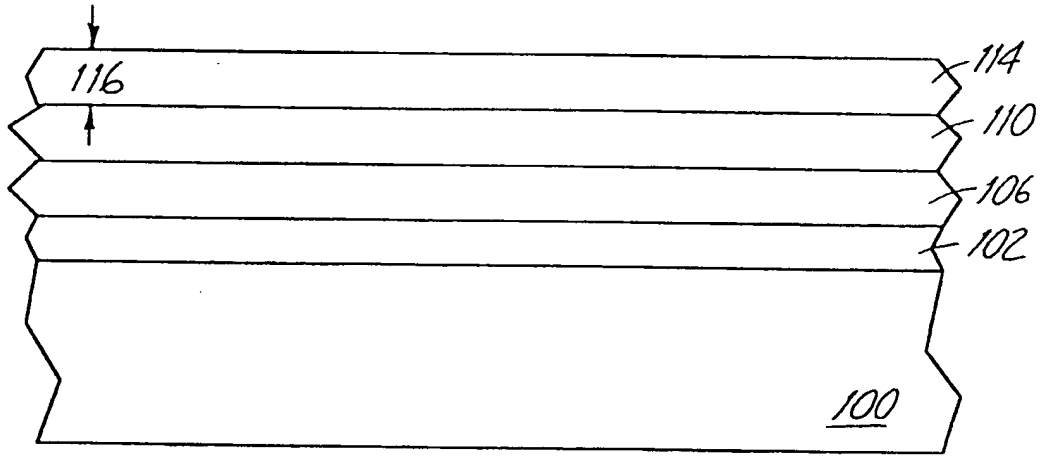

FIG. 1D

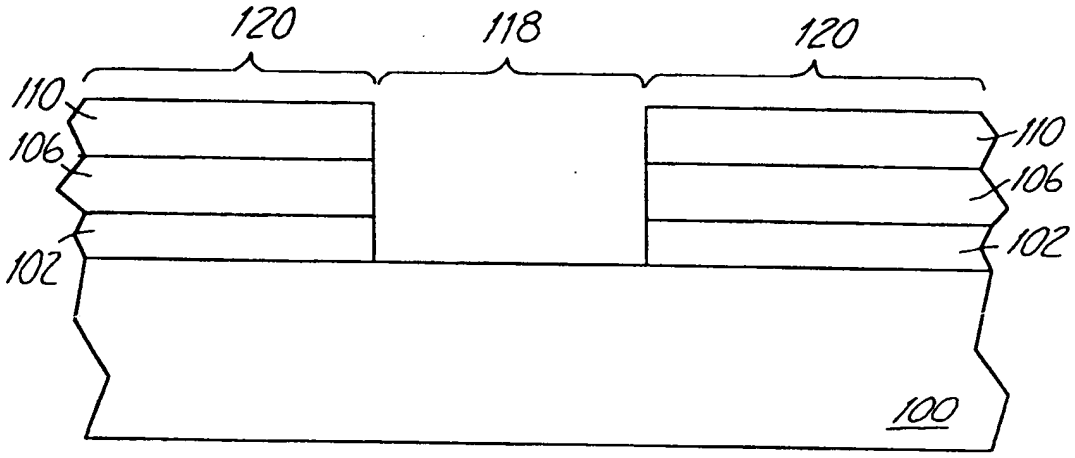
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FIG. 1E

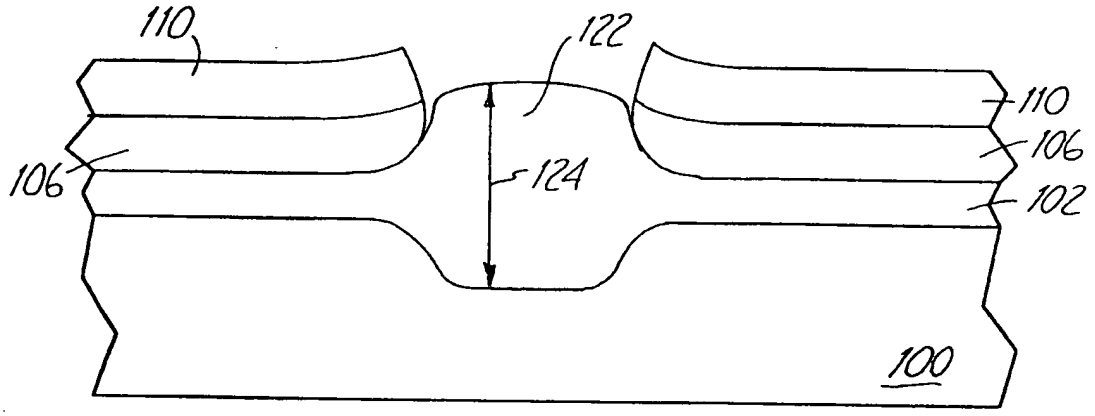
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FIG. 1F

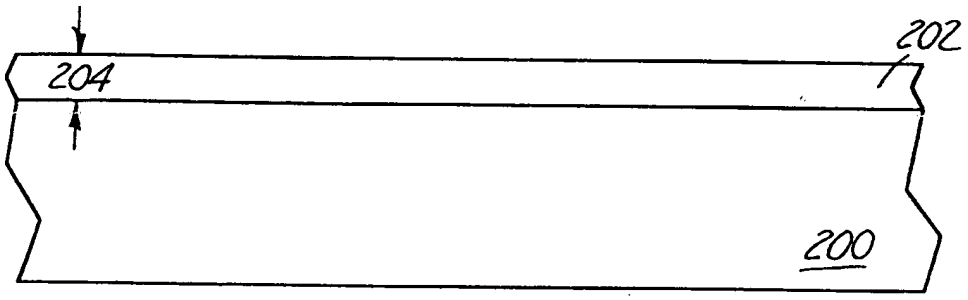

FIG. 2A

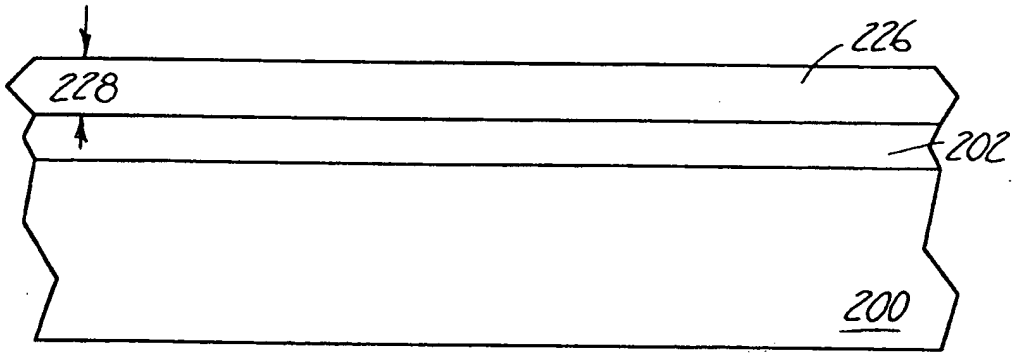

FIG. 2B

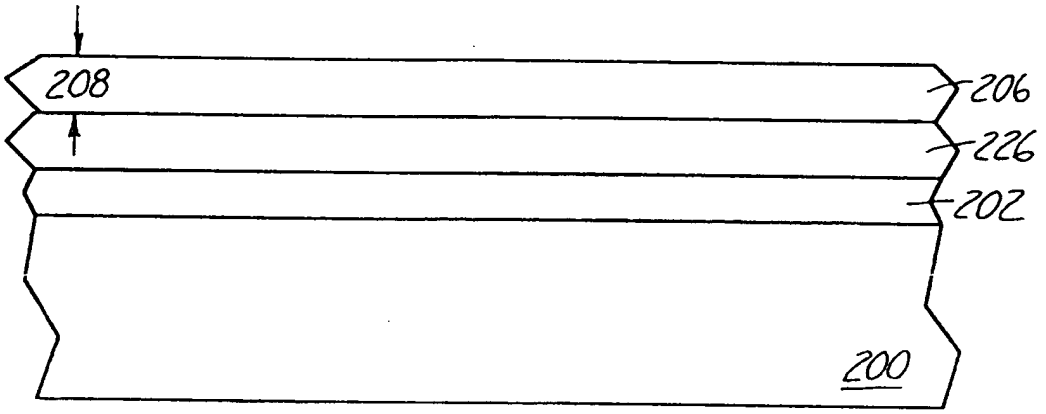

FIG. 2C

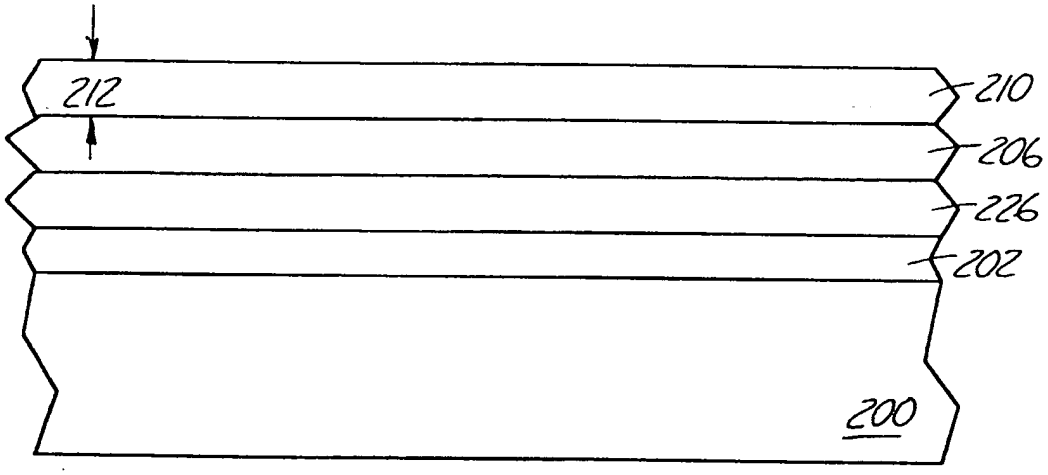

FIG. 2D

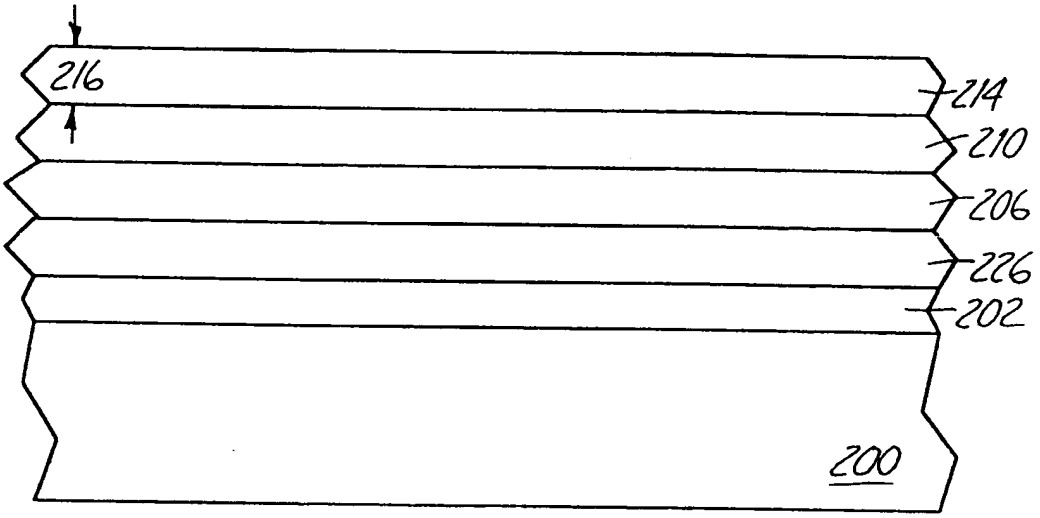
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FIG. 2E

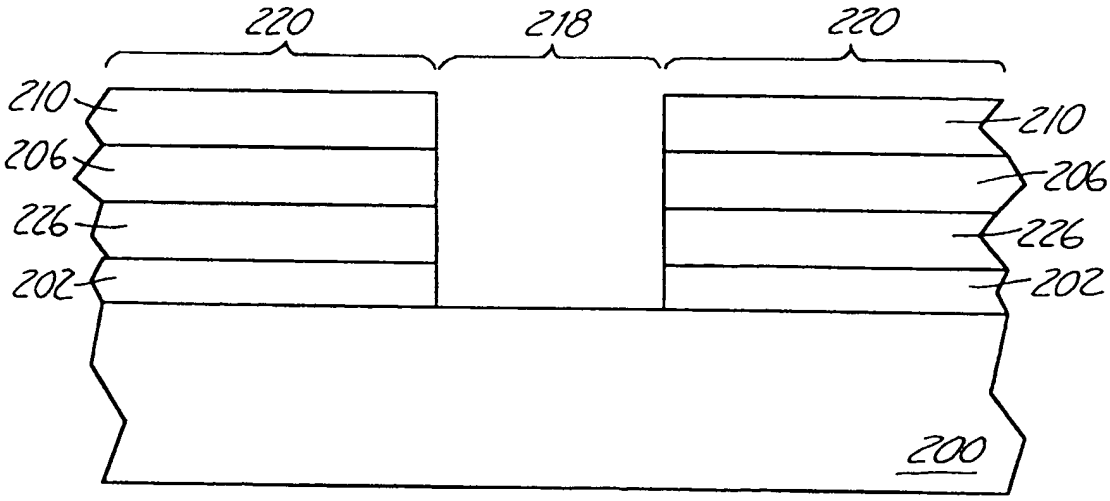
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FIG. 2F

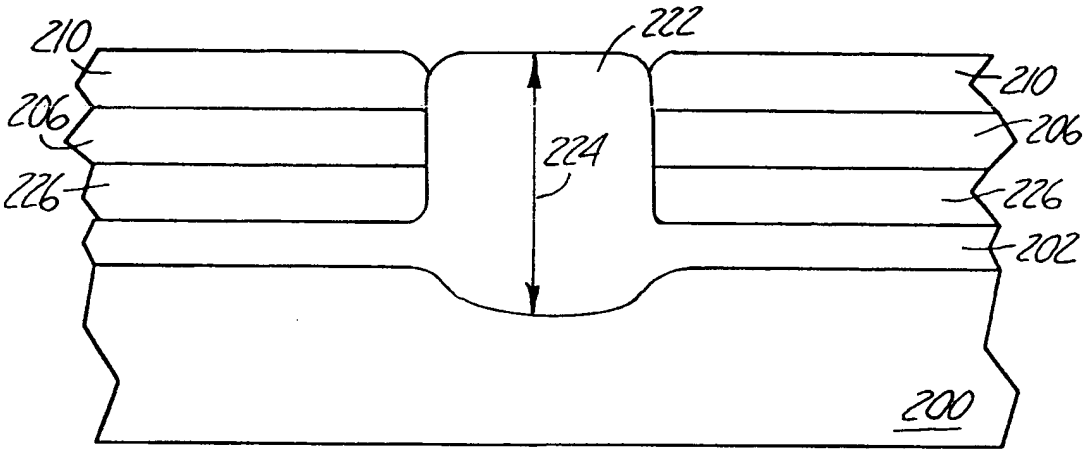

FIG. 2G

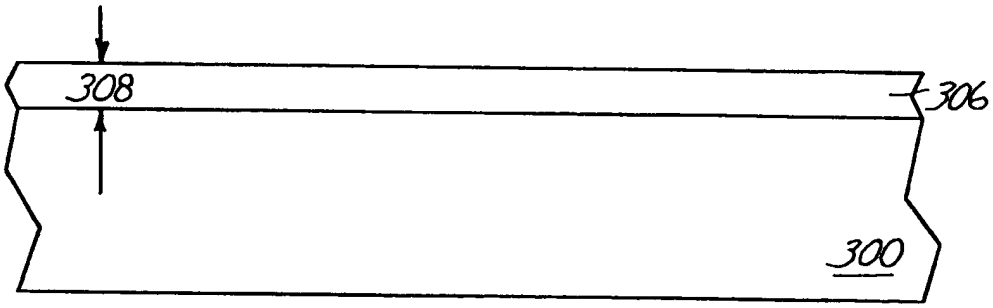

FIG. 3A

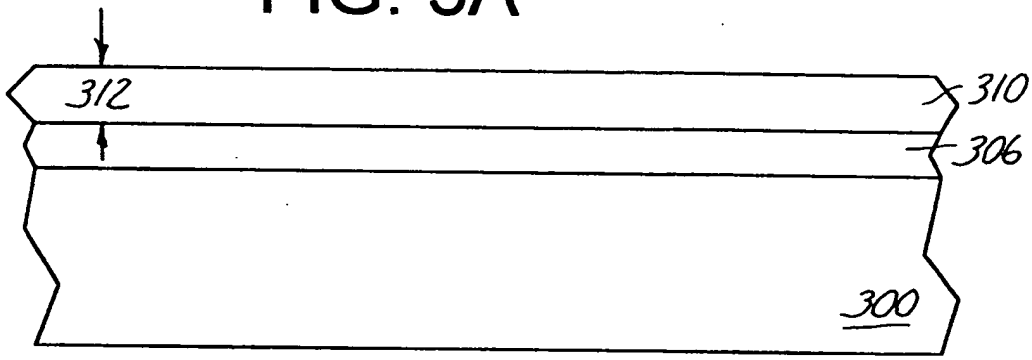

FIG. 3B

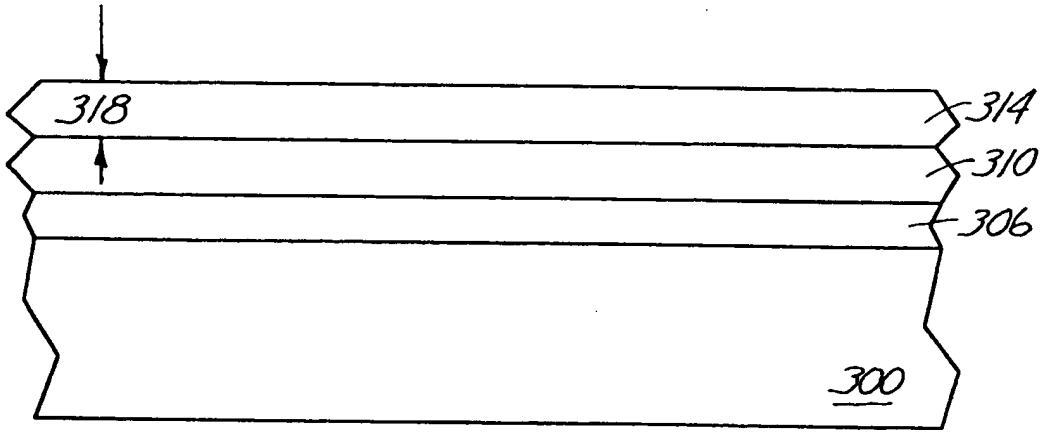

FIG. 3C

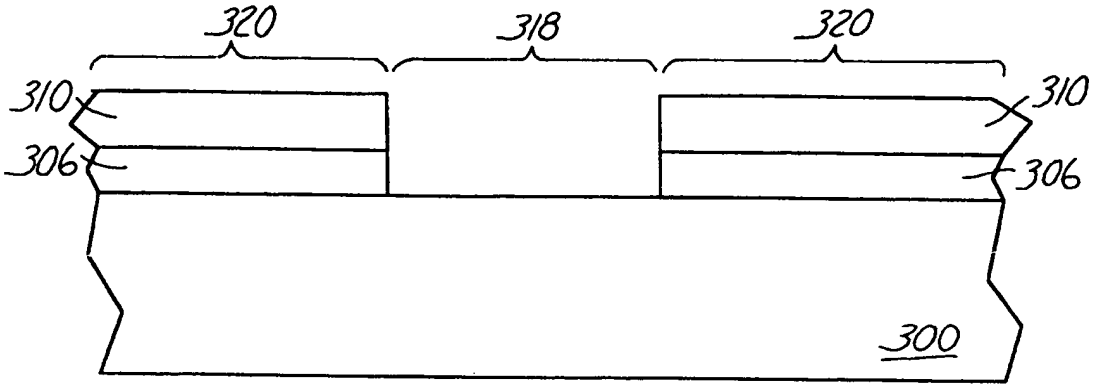

FIG. 3D

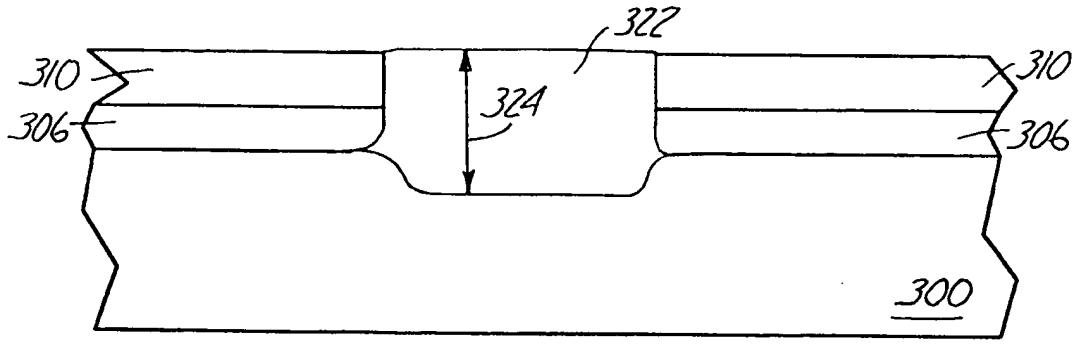

FIG. 3E

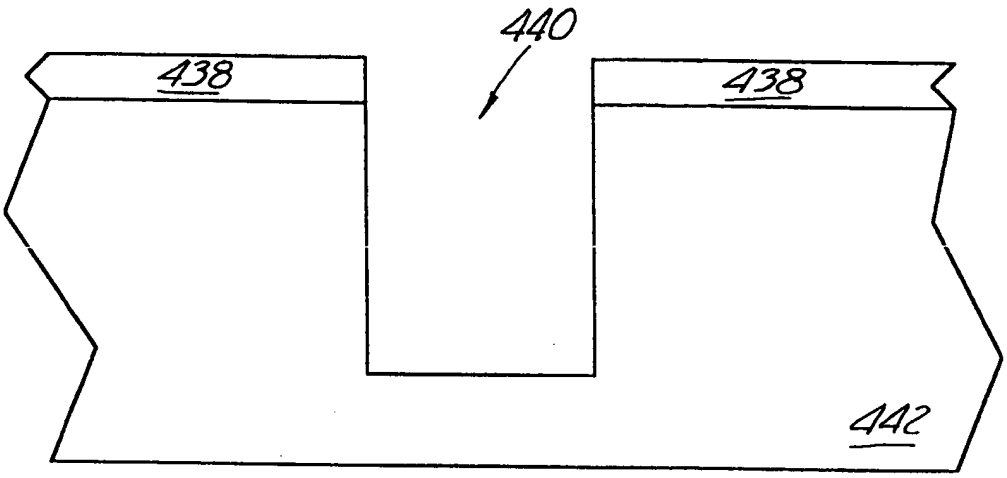

FIG. 4A

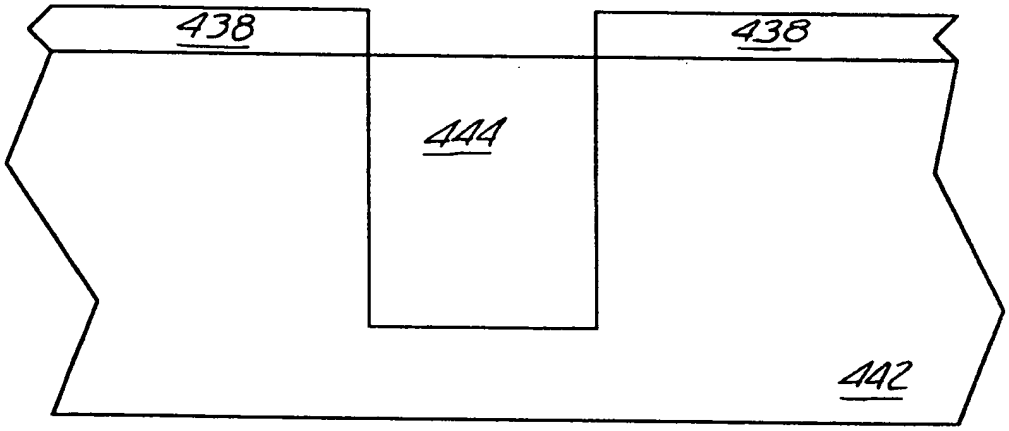

FIG. 4B

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 98/17267

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/033 H01L21/027 H01L21/762 G03F7/09

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 006, 28 June 1996 -& JP 08 031812 A (SONY CORP), 2 February 1996 see abstract	1-3, 8-11,26, 27,32, 33,35,36
Y		4-7, 12-18, 25,28, 30,34, 37,39
A		19-21, 29,38, 40,41, 43,44

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1998	30/12/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Klopfenstein, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 98/17267

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 006, 28 June 1996 -& JP 08 031811 A (SONY CORP), 2 February 1996 see abstract	1,3, 8-11,19, 20,26, 29,32, 33,36, 38,41, 42,44
Y		12-18, 21-25, 28,30, 37,39, 40,43
A		2,4-7, 10,27, 34,35, 40,43

Y	US 5 639 687 A (ROMAN BERNARD JOHN ET AL) 17 June 1997 see column 1, line 18 - line 47 see column 1, line 50 - line 65 see column 2, line 19 - column 3, line 49; figures 1-4 see column 3, line 50 - column 4, line 21; figure 5	31
A		1-4,6, 8-10, 12-14, 16,26, 28, 32-34,36

Y	PATENT ABSTRACTS OF JAPAN vol. 015, no. 288 (E-1092), 22 July 1991 & JP 03 101147 A (TOSHIBA CORP), 25 April 1991 see abstract	31

Y	TETSUO GOCHO ET AL: "CVD METHOD OF ANTI-REFLECTIVE LAYER FILM FOR EXCIMER LASER LITHOGRAPHY" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS,29 August 1993, pages 570-572, XP000409442 see page 570, paragraph 2 see page 571, paragraph 3; figures 2-4	4,5,7, 14,15, 17,21, 22,24, 34,40,43
A		6,8-10, 16,23, 26,39

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INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 98/17267

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	ONG T P ET AL: "CVD SINX ANTI-REFLECTIVE COATING FOR SUB-0.5 MUM LITHOGRAPHY" 1995 SYMPOSIUM ON VLSI TECHNOLOGY. DIGEST OF TECHNICAL PAPERS, KYOTO, JUNE 6 - 8, 1995, no. SYMP. 15, 6 June 1995, page 73/74 XP000580834 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see page 73; figure 2	4,6,14, 16,21,23
A		8-10,34, 39,40,43

Y	US 4 764 248 A (BHATTACHERJEE ARYA ET AL) 16 August 1988 see column 1, line 5 - line 9 see column 5, line 1 - line 40 see column 5, line 51 - column 6, line 46; figures 3A-3CC see column 7, line 25 - line 35 see column 7, line 56 - line 64; figures 3D-3F	30
A		1-3,7, 11-16, 26-28, 32-36

X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 224 (E-425), 5 August 1986 -& JP 61 059820 A (FUJITSU LTD), 27 March 1986 see abstract	1-3,11, 26,27, 32,33,35
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